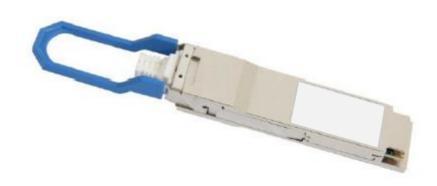


100Gbps QSFP28 Transceiver

OD-PPMQ1L410ST0

100GBASE-LR4 QSFP28 Optical Transceiver



1. Features

- Compliant to QSFP28 MSA(SFF-8665)
- Digital Diagnostic Monitoring Function (SFF-8636)
- 4 x 25G serial Interface (CEI-28G-VSR)
- Supports 106.25Gb/s bit rate
- Up to 10km over SMF (ITU-T G.652)
- Single Power Supply Voltage of +3.3V
- Hot-pluggable 38 pin electrical interface
- LC receptacle connector
- Lead-Free and RoHS Compliant

Applications
100G BASE-LR4



2. Absolute Maximum Ratings

Item	Donometer	Unit	Specification			Note
No	Parameter	Unit	Min	Тур.	Max	Note
Ab-1	Storage Temperature (Ts)	deg.C	-40	-	85	
Ab-2	Supply Voltage (Vcc1, VccTx, VccRx)	V	0	-	4.0	
Ab-3	Relative Humidity (non-condensing)	%	10	-	85	
Ab-4	Damage Threshold, each lane	dBm	5.5	-	-	

3. Operating Conditions

Item No	Items	Unit	Min.	Тур.	Max.	Remarks
Oc-1	Transmission Cable		SMF (ITU-T G.652)			
Oc-2	Case Temperature (Tc)	deg.C	0		70	
Oc-3	Power supply voltage (Vcc)	V	3.135	3.300	3.465	
Oc-4	Power Consumption	W			3.5	
Oc-5	Link Distance	km			10	

4. Block Diagram

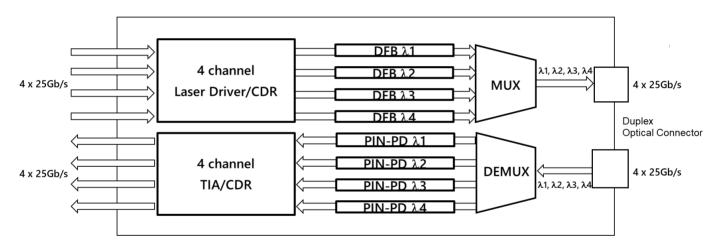


Figure 1. Block Diagram



5. Optical Interface

5.1 Transmitter Section

Item No	Parameter	Symbol	Min.	Тур.	Max.	Units	Remarks
TO-1	Aggregate Data Rate			103.125		Gb/s	
TO-2	Lane Data Rate			25.78		Gb/s	
	Center wavelength Lane 0	WL_0	1294.53	1295.56	1296.59	nm	
TO 2	Center wavelength Lane 1	WL_1	1299.02	1300.05	1301.09	nm	
TO-3	Center wavelength Lane 2	WL_2	1303.54	1304.58	1305.63	nm	
	Center wavelength Lane 3	WL_3	1308.09	1309.14	1310.19	nm	
TO-4	Total Launch Power	P_total	-	-	10.5	dBm	
TO-5	Side mode suppression ratio	SMSR	30	-	ı	dB	
TO-6	Average launch power per lane	Po_avg_ lane	-4.3	-	4.5	dBm	
TO-7	Difference in launch power between lanes		-	-	5	dB	
TO-8	Optical Modulation Amplitude (OMA), each lane	Po_OMA _lane	-1.3	-	4.5	dBm	
TO-9	Extinction ratio	ER	4	-	-	dB	
TO-10	Average launch power of off transmitter		-	-	-40	dBm	
TO-11	TDP, each lane	TDP	-	-	2.2	dB	

5.2 Receiver Section

Item No	Parameter	Symbol	Min.	Тур.	Max.	Units	Remarks
RO-1	Aggregate Data Rate			103.125		Gb/s	
RO-2	Lane Data Rate			25.78		Gb/s	
	Center wavelength Lane 0	WL_0	1294.53	1295.56	1296.59	nm	
DO 2	Center wavelength Lane 1	WL_1	1299.02	1300.05	1301.09	nm	
RO-3	Center wavelength Lane 2	WL_2	1303.54	1304.58	1305.63	nm	
	Center wavelength Lane 3	WL_3	1308.09	1309.14	1310.19	nm	
RO-4	Average receiver power per lane	Pr_avg_lane	-10.6 ⁽¹⁾	-	4.5	dBm	
RO-5	Receiver Sensitivity (OMA) per lane	Pr_OMA_lane	1	-	-8.6 ⁽²⁾	dBm	
RO-6	Difference in receiver power		-	-	5.5	dB	
RO-7	LOS Assert Level	LOSA	-24	-	-	dBm	
RO-8	LOS Deassert Level	LOSD	-	-	-14	dBm	
RO-9	LOS Hysteresis	LOSH	0.5	-	-	dB	

Note(1) Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note(2) Receiver sensitivity (OMA), each lane (max) is informative.



6. Electrical Interface

6.1 Electrical Signal Descriptions

6.1.1 ModSelL

ModSelL is an input signal. When held low by the host, the module responds to two-wire serial communication commands. The ModSelL signal allows the use of multiple modules on a single two-wire interface. When ModSelL is high, the module shall not respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input node shall be pulled towards Vcc in the module.

In order to avoid conflicts, the host system shall not attempt two-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

6.1.2 ResetL

The ResetL signal shall be pulled towards Vcc in the module. A low level on ResetL for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level of the ResetL pad is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. However, on power up (including hot insertion) the module should post this completion of reset interrupt without the host pulling ResetL low.

6.1.3 LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled toward Vcc in the module. At power-up or after ResetL is deasserted, LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the two-wire interface except during the execution of a reset. The pin is a hardware control used to put modules into a low power mode when high. When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and software control bits defines in SFF-8636, the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters. See SFF-8679 for detail description of this function.

6.1.4 ModPrsL

ModPrsL is pulled up towards Vcc_Host on the host board and pulled towards ground in the module. ModPrsL is pulled low when inserted and released to high when it is physically absent from the host connector.

6.1.5 IntL/Rx LOSL

IntL/Rx_LOSL is dual-mode active-low, open collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/Rx_LOSL is configured as IntL. If supported, IntL/Rx_LOSL can be optionally programmed as Rx_LOSL using the two-wire interface except during the execution of a reset. If IntL/Rx_LOSL is configured as IntL, a low indicates a possible module operational fault or a module condition that sets an unmasked flag as defined in SFF-8636. If IntL/Rx_LOSL is configured as Rx_LOSL, a low indicates that there is a loss of received optical power on at least one lane. "high" indicates that there is no loss of received optical power. The module shall pull Rx_LOSL to low if any lane in a multiple lane module has a LOS condition and shall release Rx_LOSL to high only if no lane has a LOS condition. See SFF-8679 for detail description of this function.



6.2 Electrical Interface Specifications

Table 1. Transmitter Electrical Specifications

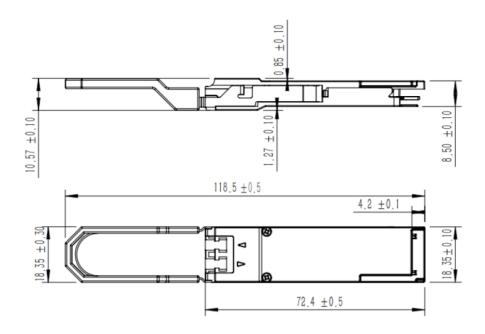
Parameter	Min.	Тур.	Max.	Units	Conditions
Signaling rate		25.78		Gb/s	CAUI-4
Differential Input voltage per lane	-	-	900	mVpp	
Input High Voltage	2	-	Vcc+0.3	V	LPMode/TxDis,
Input Low Voltage	-0.3	-	0.8	V	ResetL, ModSelL

Table 2. Receiver Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions
Signaling rate	25.78			Gb/s	CAUI-4
Differential output voltage per lane	228	-	900	mVpp	
Output High Voltage	0	-	0.4	V	ModPrsL, IntL/Rx_LOSL
Output Low Voltage	Vcc-0.5	-	Vcc+0.3	V	ModPrsL, IntL/Rx_LOSL



7. Outline Drawings 7.1 Package Outline



(Unit: mm)

Figure 2. Transceiver outline

7.2 Printed Circuit Board Connector Layout

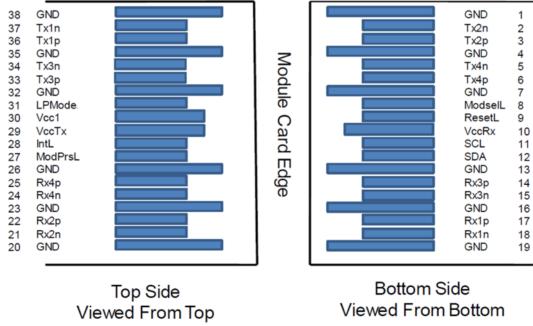


Figure 3. Pattern Layout for QSFP Printed Circuit Board



8. Pin Configuration

Table 3. Pin description

Pin No.	Symbol	Function	Plug Seq.	Notes
case	case	Module case	-	Note 1
1	GND	Ground	1st	Note 2
2	Tx2n	Transmitter Inverted Data Input	3rd	Note 5
3	Tx2p	Transmiter Non-Inverted Data Input	3rd	Note 5
4	GND	Ground	1st	Note 2
5	Tx4n	Transmitter Inverted Data Input	3rd	Note 5
6	Tx4p	Transmiter Non-Inverted Data Input	3rd	Note 5
7	GND	Ground	1st	Note 2
8	ModSelL	Module Select	3rd	Described in Section 6.1
9	ResetL	Module Reset	3rd	Described in Section 6.1
10	VccRx	+3.3V Power Supply Receiver	2nd	3.3 (+/-) 5% , Note 4
11	SCL	Two-wire interface clock	3rd	Note 3
12	SDA	Two-wire interface data	3rd	Note 3
13	GND	Ground	1st	Note 2
14	Rx3p	Receiver Non-Inverted Data Output	3rd	Note 6
15	Rx3n	Receiver Inverted Data Output	3rd	Note 6
16	GND	Ground	1st	Note 2
17	Rx1p	Receiver Non-Inverted Data Output	3rd	Note 6
18	Rx1n	Receiver Inverted Data Output	3rd	Note 6
19	GND	Ground	1st	Note 2
20	GND	Ground	1st	Note 2
21	Rx2n	Receiver Inverted Data Output	3rd	Note 6
22	Rx2p	Receiver Non-Inverted Data Output	3rd	Note 6
23	GND	Ground	1st	Note 2
24	Rx4n	Receiver Inverted Data Output	3rd	Note 6
25	Rx4p	Receiver Non-Inverted Data Output	3rd	Note 6
26	GND	Ground	1st	Note 2
27	ModPrsL	Module Present	3rd	Note 3
28	IntL/ Rx_LOSL	Interrupt/Rx_LOS	3rd	Described in Section 6.1
29	VccTx	+3.3V Power Supply Transmitter	2nd	3.3 (+/-) 5% , Note 4
30	Vcc1	+3.3V Power Supply	2nd	3.3 (+/-) 5% , Note 4
31	LPMode/ TxDIS	Low Power Mode / Tx Disable	3rd	Described in Section 6.1
32	GND	Ground	1st	Note 2
33	Tx3p	Transmiter Non-Inverted Data Input	3rd	Note 5
34	Tx3n	Transmitter Inverted Data Input	3rd	Note 5
35	GND	Ground	1st	Note 2
36	Tx1p	Transmiter Non-Inverted Data Input	3rd	Note 5
37	Tx1n	Transmitter Inverted Data Input	3rd	Note 5
38	GND	Ground	1st	Note 2

Plug Seq.: Pin engagement sequence during hot plugging.

- 1) The case makes electrical contact to the cage before any of the board edge contacts are made.
- The module signal ground contacts, GND should be isolated from the module case. GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
- SCL is the clock line of two wire serial interface for serial ID.
 SDA is the data line of two wire serial interface for serial ID.
 ModPrsL is grounded by the module to indicate that the module is present.
- 4) VccRx, VccTx and Vcc1 are the receiver, transmitter and module power supplies. They are defined as 3.3V±5% at the QSFP connector pin. These 3 pins shall be applied concurrently and may be internally connected within the module in any combination. Recommended host board power supply filtering is shown below. Inductors with DC resistance of less than 0.1 Ω should be used in order to maintain the required voltage at the host edge card connector. It is recommended that the 22uF capacitors each have an equivalent series resistance of 0.22 Ω.
- 5) Tx1p/n Tx4p/n are the differential transmitter inputs. They are AC-coupled, differential lines with 100ohm differential termination inside the module.
- 6) Rx1p/n Rx4p/n are the differential receiver outputs. They are AC coupled 100ohm differential lines which should be terminated with 100ohm (differential) at the host.

9. Recommended interface circuit

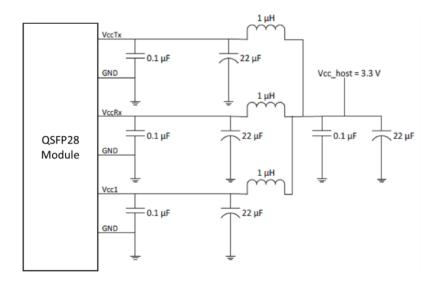


Figure 4. Recommended Host Board Supply Filtering Network



10. Digital Diagnostic Monitor Accuracy

Table 4. DDM Accuracy

Parameter	Unit	Accuracy
Tx Optical Power (Average)	dB	+/- 3 (-4.3 to 4.5dBm)
Rx Optical Power (Average)	dB	+/- 3 (-10.6 to 4.5dBm)
Bias Current	%	+/- 10
Power Supply Voltage	V	+/- 0.1
Temperature (Case)	deg.C	+/- 3

11. Label



Line 1; NEC logo

Line 2; Part Number (depend on each PN)

Line 3; Year, Month of Manufacture/2space/6-digit Serial Number

Line 4 ; Country of Manufacture

Line 5; Class 1 Laser Product

12.Ordering Information

Part Number	Fiber Optical Connector	Pull tab color	Operating Temperature Range
OD-PPMQ1L410ST0	LC	Blue	0 to 70 deg.C



- Revision history -

Revision	Date	Contents
01E	16 th March. 2023	Initial Release
02E	7 th October. 2024	Correction of typos
03E	11th December, 2024	Add Notes in 5.Optical Interface section



Area of caution

Areas of caution in the handling of laser diode products.

- •This product complies with EN 60825-1:2014 + A11:2021, IEC 60825-1:2014, IEC 60825-1:2007 and 21 CFR 1040.10, which correspond to the category "Class 1 Laser Product" under EN regulation, "Class 1 Laser Product" under IEC regulation and "Class I Laser product" under FDA regulation.
- During operations, the laser diode discharges red beams and infrared beams invisible to the eye. Since it is very hazardous if these beams directly, or bypassing through a lens, get in one's eyes, please try to avoid this.
- Take proper Electrostatic-discharge (ESD) precautions while handling the device. The device is sensitive to ESD.
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- •Be careful not to pierce your skins as the tips of optical fibers are extremely sharp. Especially you must attention in case of hazardous if they pierce one's eyes.
- Do not apply extreme stress to optical fiber, or it may cause deterioration of characteristics or disconnection. The force of pull should be less than 200gf, and a radius for bending should be larger than R30 mm
- Do not hold only optical fiber or module package, because extreme stress is easy to apply to the optical fiber edge of the module

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